REMARKS

Claims 1-4 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

Claim 2 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite.

Claim 2 has been amended to take into consideration the concerns of the Examiner.

Claims 1-4 are now in full compliance with 35 U.S.C. § 112.

Turning now to the art rejection, Claims 1-4 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kaneyama.

These rejections are respectfully traversed.

It is respectfully submitted that Kaneyama does not disclose or suggest the presently claimed invention including multiple series p-channel MOSFET input switches and multiple series p-channel MOS transistor output switches.

Figure 3 of Kaneyama only shows n-channel devices.

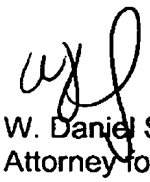
In light of the above, it is respectfully submitted that Claims 1-4 patentably define over the applied art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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